T05-T50-C84-2D6-60

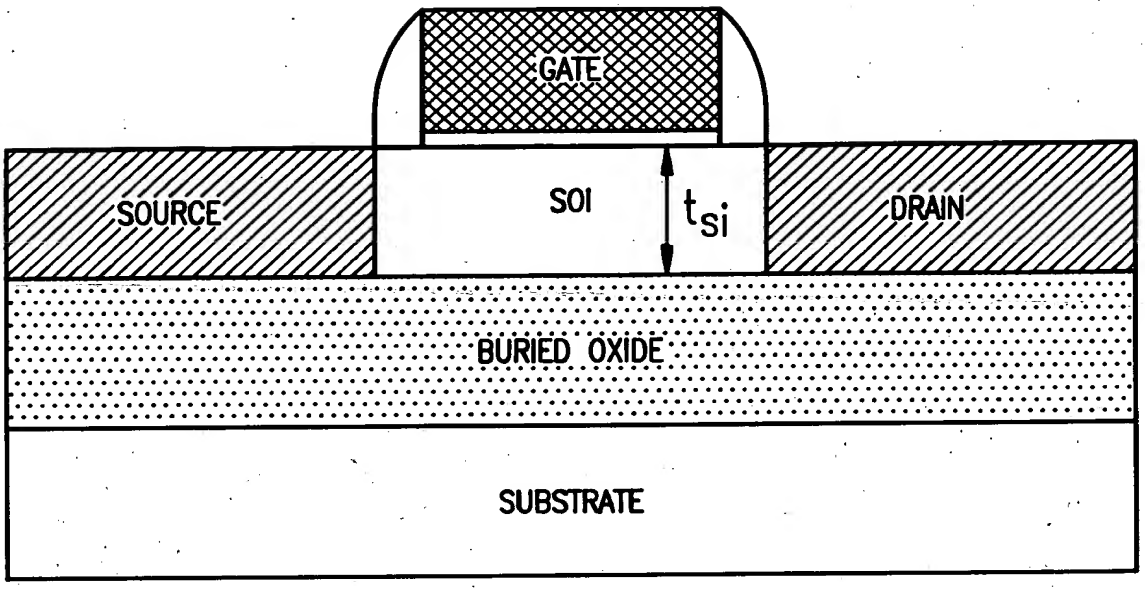


FIG.1

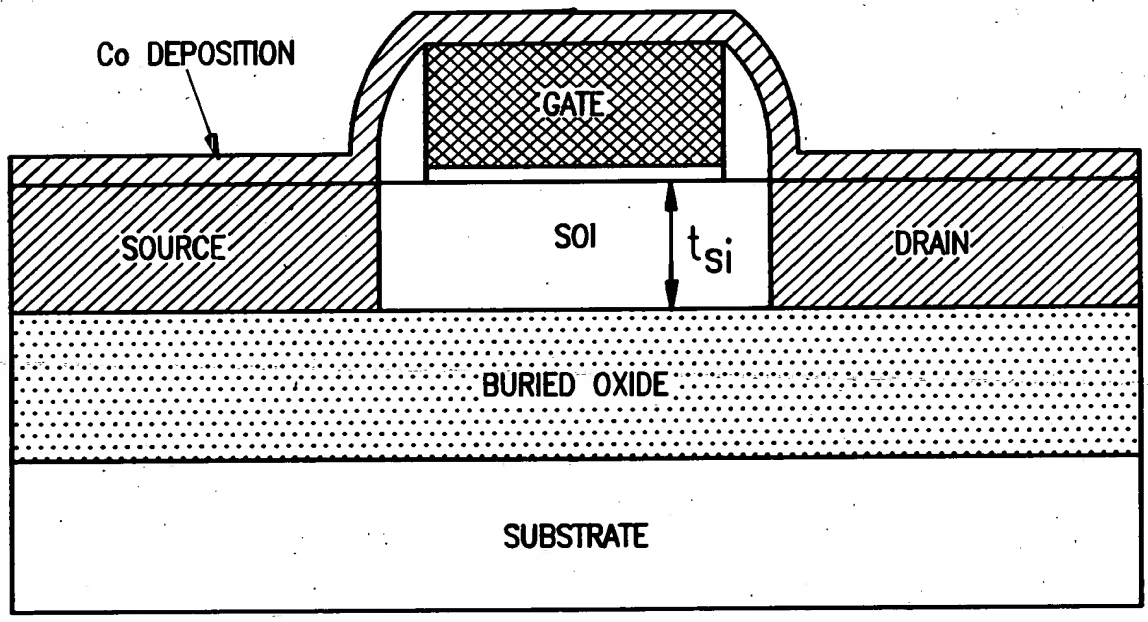


FIG.2

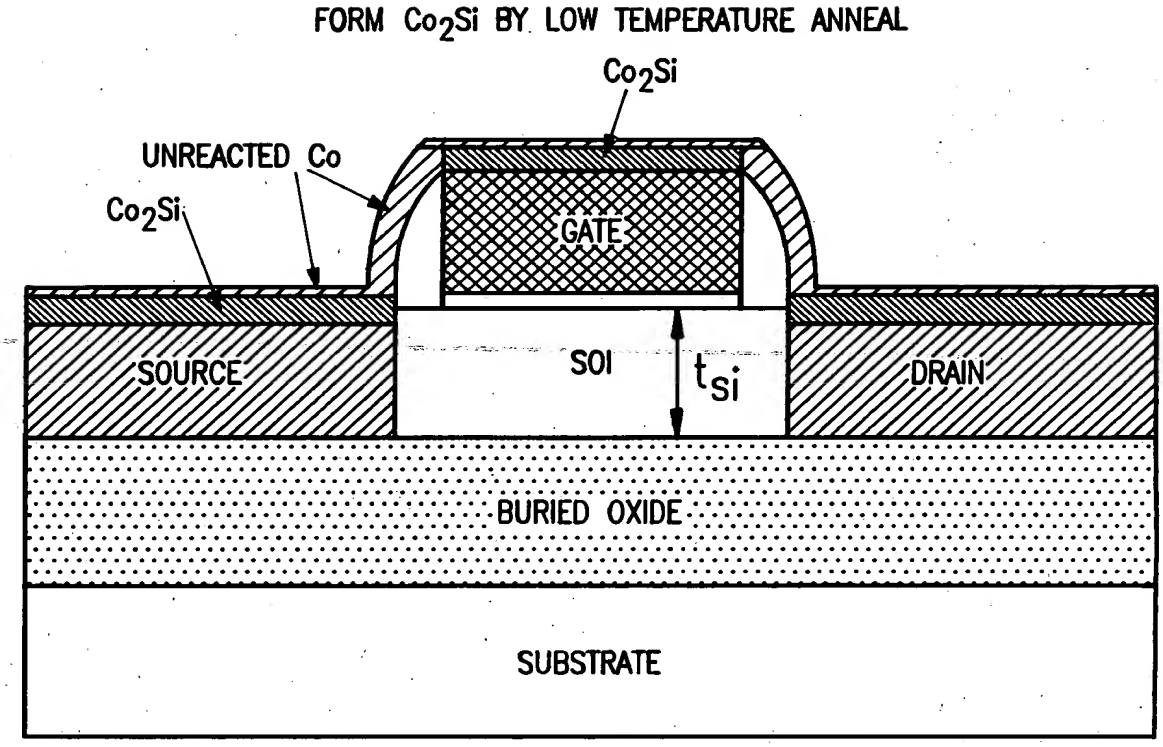


FIG.3

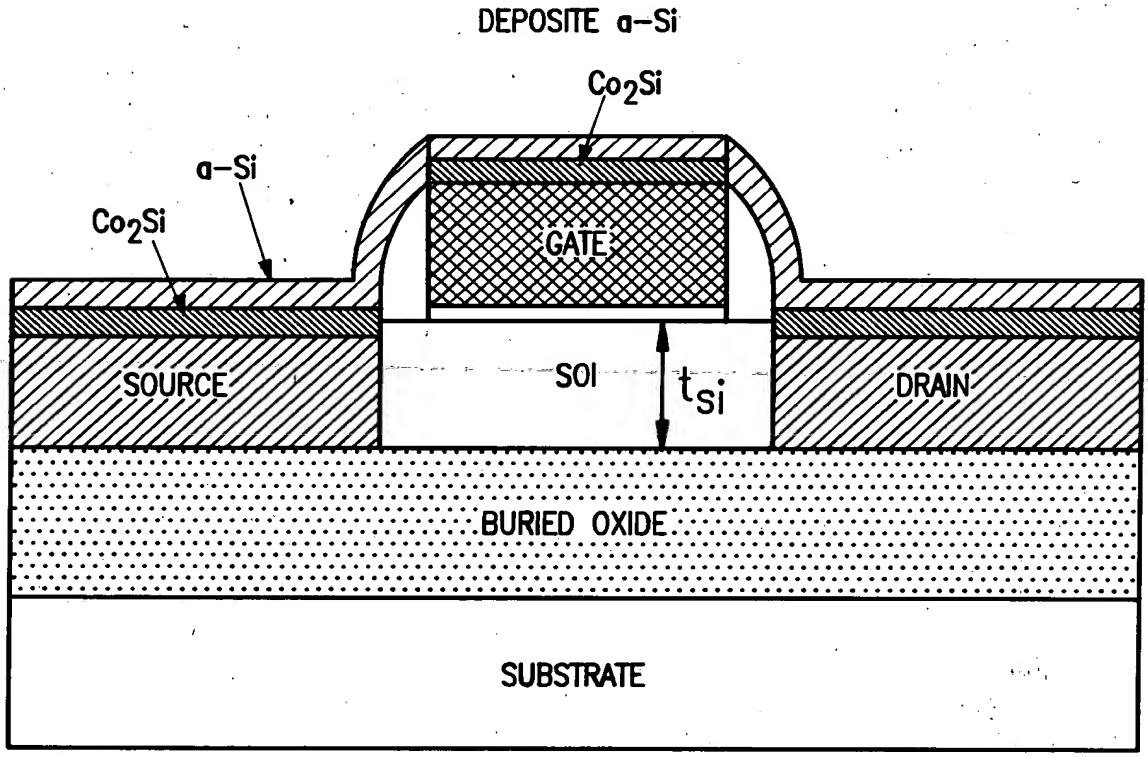


FIG.4

FOR TECHNOLOGY DEVELOPMENT

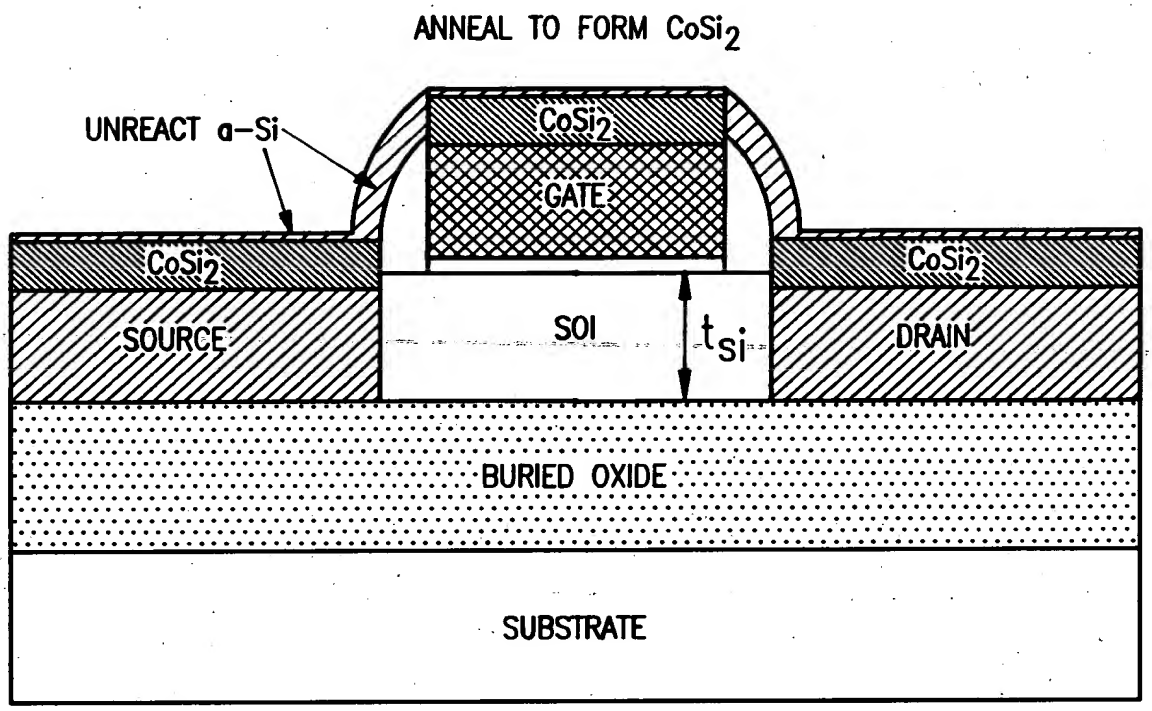

ANNEAL TO FORM $CoSi_2$
UNREACT a-Si
$CoSi_2$
GATE
$CoSi_2$
$CoSi_2$
SOURCE
SOI
t_{Si}
DRAIN
BURIED OXIDE
SUBSTRATE

FIG.5

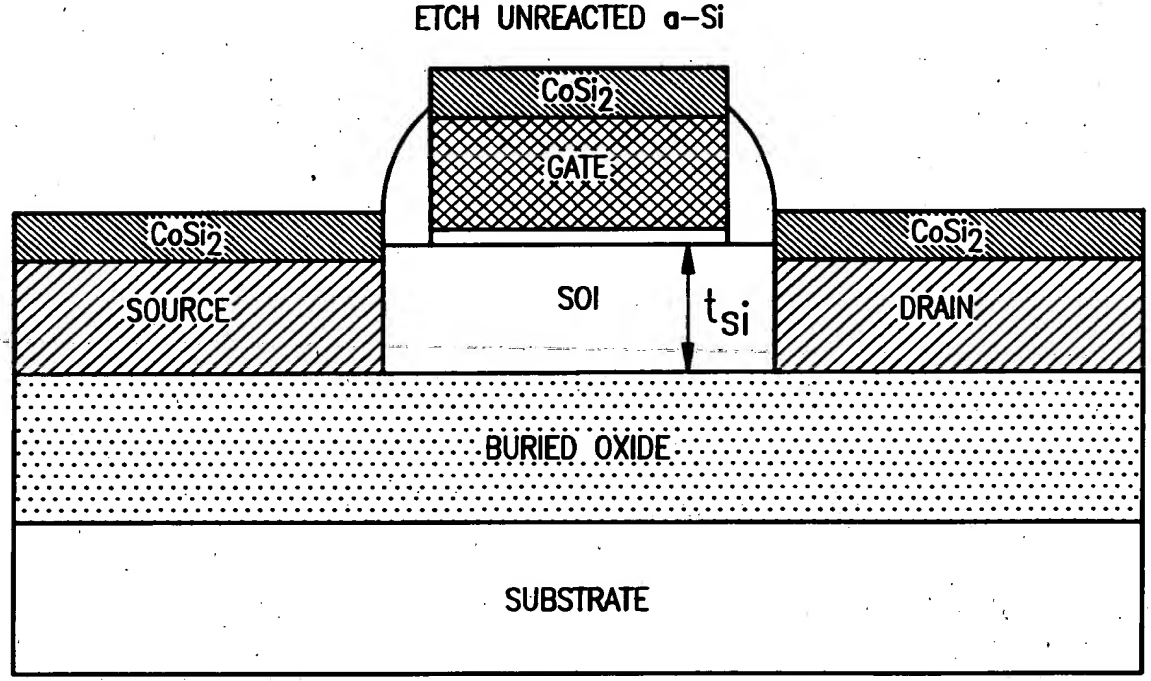

ETCH UNREACTED a-Si
$CoSi_2$
GATE
$CoSi_2$
$CoSi_2$
SOURCE
SOI
t_{Si}
DRAIN
BURIED OXIDE
SUBSTRATE

FIG.6

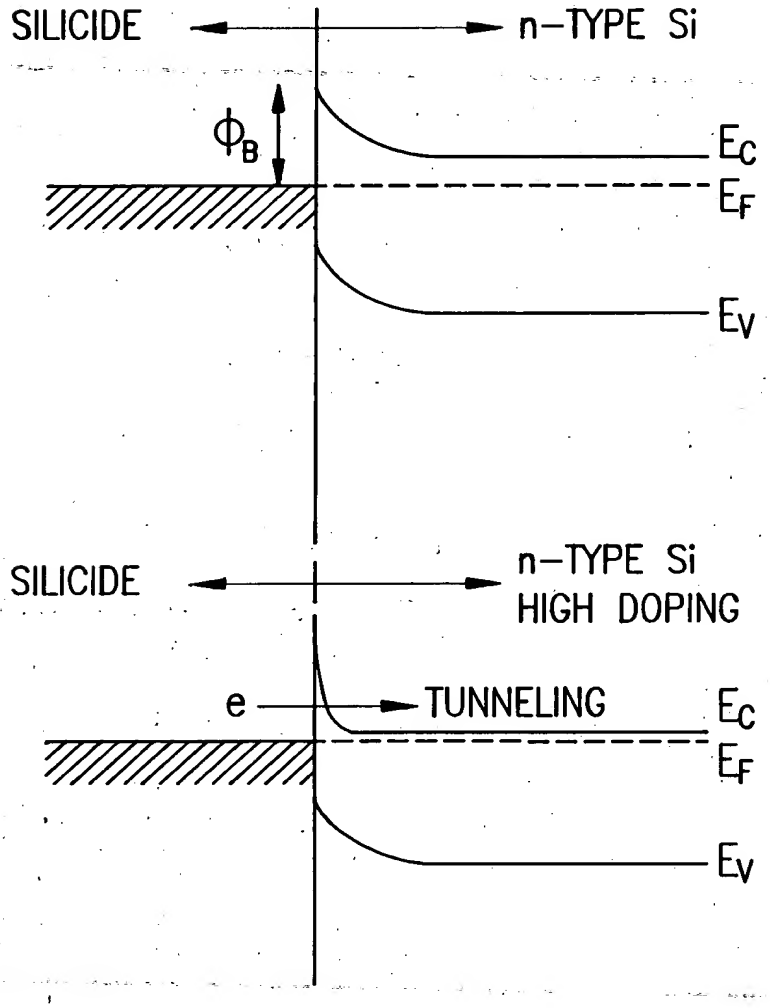
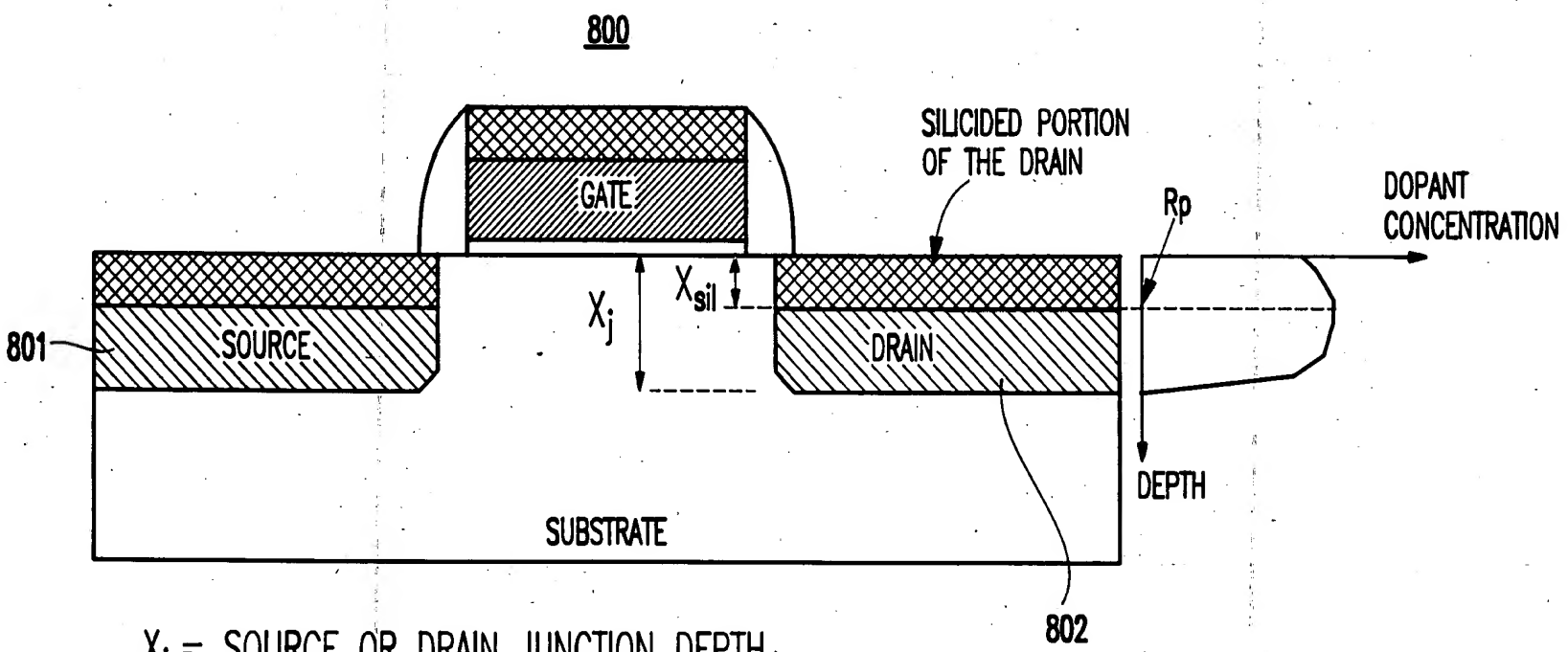

SILICIDE
n-TYPE Si
Φ_B
E_C
E_F
E_V

FIG.7A

SILICIDE
n-TYPE Si
HIGH DOPING
e
TUNNELING
E_C
E_F
E_V

FIG.7B

T0660 E8h20660



X_j = SOURCE OR DRAIN JUNCTION DEPTH

X_{sil} = SILICIDE JUNCTION DEPTH

Rp = PEAK DOPANT CONCENTRATION

REQUIREMENTS:

1. $X_j > X_{sil}$
2. X_{sil} ROUGHLY EQUALS Rp

FIG.8

T0660 E8h20660

FIG.9A

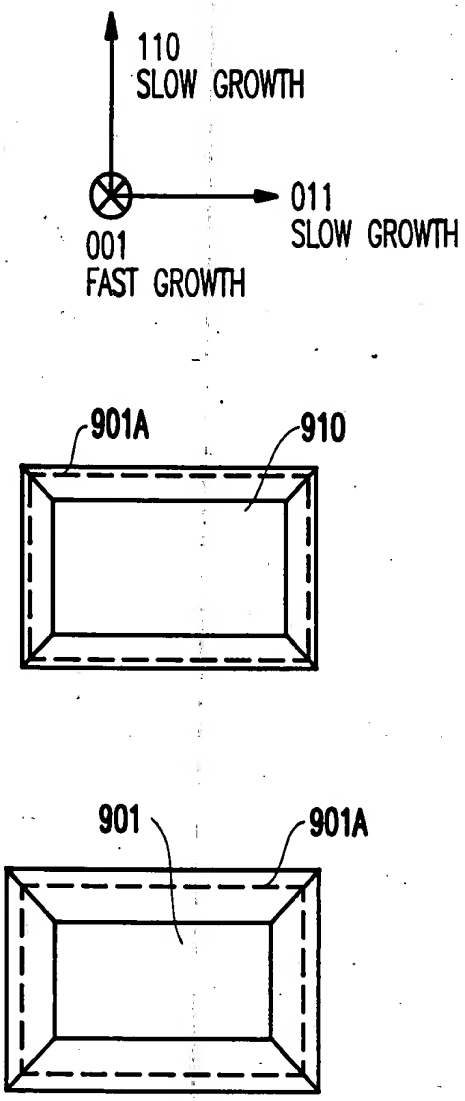
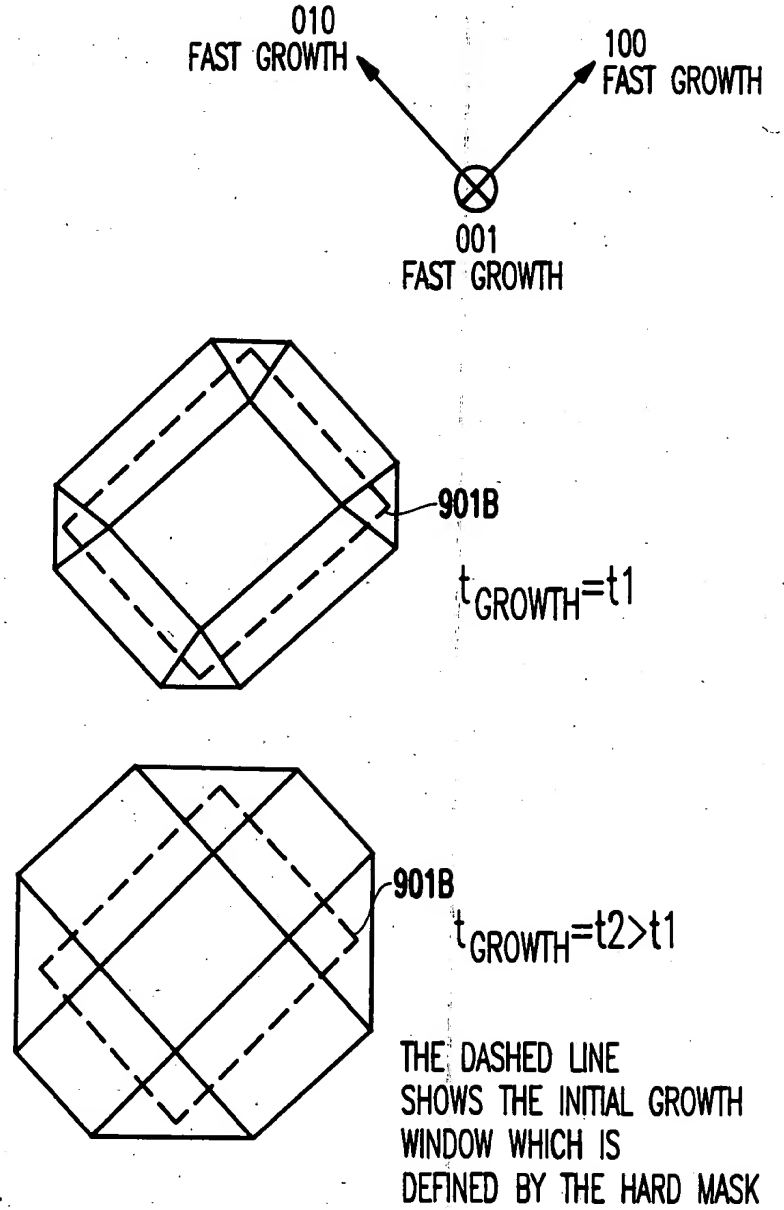



FIG.9B